

WHAT IS CLAIMED IS;

1 1. A method for the formation of rectifying junctions on alloy-semiconductors
2 comprising the steps of:
3 photo-electrochemical removal of one component of the alloy material and
4 chemical etching of another component of the alloy
5 to produce a positive-intermediate-negative (PIN) structure semiconductor.

1 2. The method according to Claim 1, wherein the alloy semiconductor comprises
2 a combination of Group II element and a Group VI element.

1 3. The method according to Claim 2, wherein the alloy semiconductor comprises
2 CdTe.

1 4. The method according to Claim 2, wherein the alloy semiconductor comprises
2 CdZnTe.

1 5. The method according to Claim 2, wherein the alloy semiconductor comprises
2 HgZnCdTe.

1 6. The method according to Claim 2, wherein the alloy semiconductor comprises
2 HgCdZnSe.

1 7. A method for the formation of rectifying junctions on alloy-semiconductors
2 comprising the steps of:
3 photo-electrochemical removal of one component of the alloy material to produce one
4 portion of the junction and
5 deposition of a second component to produce a second portion of the junction
6 to produce a positive-intermediate-negative (PIN) structure semiconductor.

1 8. The method according to Claim 7, wherein the alloy semiconductor comprises
2 a combination of Group II element and a Group VI element.

1 9. The method according to Claim 8, wherein the alloy semiconductor comprises
2 CdTe.

1 10. The method according to Claim 8, wherein the alloy semiconductor comprises
2 CdZnTe.

1 11. The method according to Claim 8, wherein the alloy semiconductor comprises
2 HgZnCdTe.

1 12. The method according to Claim 8, wherein the alloy semiconductor comprises
2 HgCdZnSe.

1 13. A positive-intermediate-negative (PIN) structure semiconductor constructed
2 by the process consisting of the steps of:
3 photo-electrochemical removal of one component of the alloy material and
4 chemical etching of another component of the alloy
5 to produce the positive-intermediate-negative (PIN) structure semiconductor.

1 14. The PIN structure semiconductor according to Claim 13, wherein the alloy
2 semiconductor comprises a combination of Group II element and a Group VI element.

1 15. The PIN structure semiconductor according to Claim 14, wherein the alloy
2 semiconductor comprises CdTe.

1 16. The PIN structure semiconductor according to Claim 14, wherein the alloy
2 semiconductor comprises CdZnTe.

1 17. The PIN structure semiconductor according to Claim 14, wherein the alloy
2 semiconductor comprises HgZnCdTe.

1 18. The PIN structure semiconductor according to Claim 14, wherein the alloy
2 semiconductor comprises HgCdZnSe.

1 19. A device for detecting and measuring an electrical response due to a single
2 charge carrier in a room-temperature semiconductor, the device comprising:

3 a PIN structure semiconductor, said semiconductor having first and second ends;

4 a first electrode in electrical contact with said first end, said first electrode biased at a
5 first electrical potential;

6 a second electrode in electrical contact with said second end, said second electrode
7 biased at a second electrical potential, said first potential greater than said second potential;

8 wherein the PIN structure semiconductor is constructed by the process consisting of
9 the steps of:

10 photo-electrochemical removal of one component of the alloy material and

11 chemical etching of another component of the alloy

12 to produce the PIN structure semiconductor.

1 20. The device according to Claim 19, wherein the alloy semiconductor comprises
2 a combination of Group II element and a Group VI element.

1 21. The device according to Claim 20, wherein the alloy semiconductor comprises
2 CdTe.

1 22. The device according to Claim 20, wherein the alloy semiconductor comprises
2 CdZnTe.

1 23. The device according to Claim 20, wherein the alloy semiconductor comprises
2 HgZnCdTe.

1 24. The device according to Claim 20, wherein the alloy semiconductor comprises
2 HgCdZnSe.

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